IN THE SPECIFICATION

Please amend the paragraph in the specification on page 1, beginning on line 8 as follows:

This application is a continuation of commonly assigned U.S. Patent Application Nos. 10/098,652, 10/098,255 and 10/098,990 all filed March 14, 2003 which are continuations-in-part of commonly assigned U.S. Patent Application Nos. 09/896,513, 09/896,664, 09/896,196 and 09/896,192, all filed June 29, 2001 and which are all incorporated herein by reference in their entirety.

Please amend the paragraph in the specification on page 5, beginning on line 19 as follows:

Some have attempted to make two-dimensional fiber bundle arrays ~~for~~ by creating a dense packing of fibers together, for example, as described in U.S. Patent 5,473,716, and K. Koyabu, F. Ohira, T. Yamamoto, "Fabrication of Two-Dimensional Fiber Arrays Using Microferrules" IEEE Transactions on Components, Packaging and Manufacturing Technology—Part C, Vol 21, No 1, January 1998. However, these attempts have not yielded a solution, particularly for the types of connectors mentioned above, because the inaccuracies of fiber production result in diameters of fibers which fluctuate within a 2 micron range (i.e. plus or minus 1 micron). Hence if 12 fibers are stacked in a row, there could be as much as 12 microns of inaccuracy in fiber alignment. Even with multi-mode fibers (the best of which use 50 micron cores), a misalignment of 12 microns will cause unacceptable light loss for most applications. For single mode fibers, which typically have 9 micron diameter cores, a 7 to 12 micron misalignment could mean that, irrespective of the alignment of the fiber at one end of the row, entire fibers at or near the other end of the row could receive no light whatsoever. For two-

dimensional fiber arrays, the problem is even worse because the inaccuracy of the fiber is not limited to one direction. Thus, for example with a 16 x 16 array, a plus or minus 1 micron inaccuracy could result in fiber misalignments by up to 23 microns or more. Compounding the problem is the further fact that fiber inaccuracies stated as plus or minus 1 micron do not mean that fiber manufacturers guarantee that the fiber will be inaccurate by no more than 1 micron. Rather, the inaccuracy statement represents a standard deviation error range. This means that most of the fiber should only be that inaccurate. Individual fibers, or portions thereof, could have larger inaccuracies due to statistical variations.

Please amend the paragraph in the specification on page 12, beginning on line 11 as follows:

Advantageously, the technique is scalable, permitting concurrent manufacturing of multiple such devices on individual wafers, irrespective of wafer diameter, the only limitations being the ~~due to~~ number and size of the devices that will fit within a wafer's area and/or the number of wafers that can be concurrently etched and/or oxidized. Such limitations however, are independent of the invention.

Please amend the paragraph in the specification on page 21, beginning on line 18 as follows:

a) The wafer is processed into a series of chips by etching holes through the wafer using either an etching or drilling process. In some variants, this is done through a semiconductor lithography process combined with an etching technique. In other variants, laser drilling is used. The holes are each of specific sizes and, where appropriate, axially offset at a specific angle relative to the plane of the wafer (or piece once cleaved). Features such as holes for alignment pins or bumps and recesses for precision mating are also created, where

appropriate. The wafer contains many copies of the chips that will be needed to make a particular high precision piece, for example, fiber holding piece, a collimator, many-to-one taper or Y branch. The pieces to build up an element of a particular type can be processed on a single wafer or by making several wafers, each having some of the pieces needed to make the component. In either case, the resultant wafer scale batch processing is the same and saves costs.

Please amend the paragraph in the specification on page 22, beginning on line 8 as follows:

The holes are classified into two groups: those which are made for fiber insertion and/or receiving an optical epoxy, and those that are for alignment and/or placement into a connector. Although in the ideal case, the holes are perfectly cylindrical, frustoconical, obconic or funnel shaped, in practice the holes ~~will~~ may only be substantially ~~right~~ cylindrical, ~~right~~ frustoconical or ~~right~~ funnel shaped. However, those deviations, for purposes of the processes described herein, are considered negligible since they are either a) much smaller than the optical fiber diameter and hence have no meaningful effect on placement or performance in the case of fiber holding embodiments, or (b)virtually irrelevant in the case of waveguide embodiments.

Please amend the paragraph in the specification on page 24, beginning on line 3 as follows:

In some variants using straight holes, the holes are created by laser drilling. In other variants, the straight holes are formed using an etching process, for example, anisotropic hole etching. By way of example, for a silicon wafer, anisotropic deep/via hole etching of silicon is performed by photoresist patterning the wafer according to the desired hole placement and etching using the Bosch process in a high-density plasma reactor such as either an electron cyclotron resonance (ECR) or inductively coupled plasma (ICP) reactor. The Bosch process is

based off of a time multiplexing scheme separating the etch (SF6) and passivation (C4F8 sidewall protection) cycles. The etch causes scalloping on the silicon sidewalls and sharp edges at the base of the via but the profile produces nice straight holes/vias. Since the scalloping creates edges that are too sharp for fiber insertion without a guiding structure to help the fiber avoid the edges at the base of the structure, clean-up etching is required.

Please amend the paragraph in the specification on page 29, beginning on line 10 as follows:

In the male version of the connector the alignment pins are permanently inserted into the connector. In the female version of the connector, the pins are removed. When a male and female connector are joined, if the connector contains a female ~~format~~ side high precision piece, the alignment pins in the male ~~format~~ side of the connector slot through the high-precision piece holes into the holes in the female ~~format~~ side low-precision piece. The high precision piece is thin and strong but brittle, so that, for the female piece, repeated alignment pin insertion results in increased stress during connector combining that can ultimately cause the high precision piece to crack.

Please amend the paragraph in the specification on page 29, beginning on line 18 as follows:

Since the holes in the low-precision piece alone can supply the required accuracy in mating male and female pieces, and provide the necessary strength in connection, the alignment pin holes in the high-precision piece are not essential for proper operation. Their primary function is for accurately placing the high-precision piece into the low-precision piece. Once the high precision piece has been affixed to the low-precision piece, the need for the alignment pin holes in the high precision piece is eliminated. Thus, to avoid creating a cracking problem, the

general procedure described above is slightly different for creating a female ~~format~~ side connector than for creating a male ~~format~~ side connector. In overview, the procedure is as follows:

Please amend the paragraph in the specification on page 30, beginning on line 5 as follows:

A low-precision ~~pieces~~ piece in which the spacing accuracy of the alignment pin holes, and the depth into which the alignment pins will insert into those holes, is sufficient to align and hold a connector together even if no high precision piece were present, is created.

Please amend the paragraph in the specification on page 31, beginning on line 1 as follows:

For a male side ~~format~~ connector, the alignment pins are left in-place. For a female side ~~format~~ connector, the alignment pins are removed.

Please amend the paragraph in the specification on page 31, beginning on line 3 as follows:

Female side ~~format~~ pieces are then further processed by modifying the alignment pin holes of the ferrule so the high precision piece is not overstressed by repeated attaching and detaching of a connector. Thus, for a female piece only, the alignment pin holes, in only the high precision piece, are either:

Please amend the paragraph in the specification on page 32, beginning on line 13 as follows:

Fibers are inserted through the low-precision piece and then through the high precision piece so as to terminate in, or just beyond the outer face of the high precision piece. The low-precision piece then is filled with epoxy to hold the fibers in place via, for example, an inlet

formed in the piece. If desired, the combined unit can then be polished so that the ends of the fibers are flush with the face (i.e. the front) of the combined piece or slightly protruding. Optionally, the face of the piece where the fibers are visible can be coated with a diamond thin film (or other hard material) to prevent the silicon from being worn down during the polishing process.

Please amend the paragraph in the specification on page 33, beginning on line 2 as follows:

In order to have accurate fiber placement, the wafers that are used are typically relatively thick, for example, at least the thickness of an optical fiber or about 100 microns. However, holes that will receive optical fibers must be accurate, in diameter or in their narrowest dimension in the case of non-round or oval holes, to approximately 1 micron. In some variants however, this tolerance is extremely tight and can be difficult to consistently achieve from wafer run to wafer run and/or to maintain with consistency across entire wafers, which presently range from 4 to 12 inches in diameter, for silicon wafers.

Please amend the paragraph in the specification on page 42, beginning on line 8 as follows:

First, the appropriate guiding structures (cavities) are pattern etched in the wafer, typically a silicon wafer. Then the wafer is treated with a reactive gas, in the case of silicon, to for example, oxidize the exposed surface, which creates a relatively low refractive index cladding layer on the surface of the cavities. Alternatively, different reactive gasses can be used that will turn the silicon into an oxy-nitride or a nitride. Then the remaining cavity is filled with a high refractive index material, for example, epoxy. Further optional processing can then be performed such as etching any excess epoxy, polishing, cleaving and/or stacking as necessary.

Please amend the paragraph in the specification on page 46, beginning on line 20 as follows:

The first of the two, the through-hole format of FIG. 40D, involves taking a wafer (FIG. 40A), for example, a silicon wafer, and making holes in it (FIG. 40B), for example, straight, angled tapered, oval, etc. holes made by etching, drilling, ~~or~~ micromilling, etc. the wafer so that the holes go through the piece, for example, in a one- or two dimensional array.

Please amend the paragraph in the specification on page 47, beginning on line 9 as follows:

Once the holes have been made, in this case etched, the etched holes are turned into guiding structures by treating the wafer with a reactive gas to change the holes into a lower refractive index material to act as cladding (FIG. 40C), for example, for silicon by treating with steam at a high temperature in this case by oxidizing the silicon wafer to create the cladding layer of silicon dioxide (SiO_2), followed at some point by filling the holes with a material with a higher refractive index than the cladding, e.g. in the example case polyimide or an optical epoxy (FIG. 40D).

Please amend the paragraph in the specification on page 47, beginning on line 13 as follows:

In the waveguide format, several layers of wafers will almost always be stacked to make, for example, a two dimensional array. However, unlike with the through-hole format, the guide structures run along the surface of the wafer, such as shown in FIG. 41. This requires extremely precise spacing of wafers in the vertical dimension (FIG. 41A), particularly where, at the input or output side of the guide device, a precise pitch must be maintained. Advantageously, since

silicon wafers of precise standard thicknesses, for example 250 microns, are readily available and have extremely tight tolerances on both the overall thickness and thickness uniformity, this thickness can be used to accurately space the wafers in the vertical dimension while the precision lithography techniques maintain accuracy in the horizontal dimension. In other words, in contrast to prior art techniques that ~~patter~~ pattern waveguides on the silicon wafer, waveguide structures, like trenches or grooves, are made into the surface of the wafer, for example by etching or micromilling (FIG. 41B), so that wafers (or pieces thereof) can be stacked top to bottom with consistent wafer tolerance level accuracy.

Please amend the paragraph in the specification on page 48, beginning on line 4 as follows:

To make the waveguide format, trench structures are made into the surface of the wafer (FIG. 41B) and then the wafer is treated with a reactive gas to create a lower refractive index cladding on the surface of the material and thereby form a cladding layer on that surface (FIG. 41C), in the case of silicon it is oxidized into silicon dioxide. Optionally, cladding on the upper surface can be polished off (FIG. 41C). A core material coat that has a higher refractive index than the cladding is added, for example, a high-index material, like polyimide, is then put into the formed structures (FIG. 41D) and then any excess high-index material that may extend above or be on the top of the wafer is removed, for example by etching, polishing or other process (FIG. 41E). Optionally, if a metal-to-metal fusion process is to be used, a very thin metal layer is deposited on at least the back of the wafer (FIG. 41F). An appropriate number of wafers 4150 and, if necessary, a suitably treated or oxidized "cap" layer 4152 are then stacked and bonded together (FIG. 41G) by (for example) a wafer fusion process.